

Docket No. 11675.76.1.1

of

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and

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for

INTERLEVEL DIELECTRIC STRUCTURE

AND METHOD OF FORMING SAME

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1 nothing (a vacuum) between them is known as the dielectric constant of the given material.
2 Thus a material with a high dielectric constant placed between two conductors increases the
3 capacitance between the two conductors.

4 The increasing density of integrated circuits has resulted in unneeded capacitance
5 between metal lines in an integrated circuit due to metal line coupling capacitance. The
6 unneeded capacitance slows circuit performance by causing too much buildup of charge
7 where none is needed, thus slowing the buildup of charge at circuit elements where it is
8 needed.

9 *sub 02* One way to decrease unneeded capacitance between metal lines in an integrated
10 circuit is to decrease the dielectric constant of the material between them. Silicon dioxide,
11 the material of choice for interlevel dielectrics, has a relatively high dielectric constant.
12 Replacing silicon dioxide with a material having a lower dielectric constant would thus
13 provide reduced capacitance. Useable materials having a low dielectric constant (e.g. less
14 than about 3.6.) are generally much less stable than silicon dioxide and are thus unable to
15 reliably protect the metal lines, and are ~~unable withstand further processing.~~

16 *sub 03* One way to gain some of the benefits of low dielectric constant materials is shown
17 in Figure 1. Figure 1 is a partial cross section of a partially formed integrated circuit
18 device. A substrate or lower layer 12 has a first dielectric layer 14 comprised of a traditional
19 dielectric material such as silicon dioxide. Lines of conductive material 16, typically metal,
20 overlie first dielectric layer 14. A material with a dielectric constant lower than that of
21 silicon dioxide 18 is located in between lines of conductive material 16. Lines of conductive
22 material 16 together with low dielectric constant dielectric material 18 are covered by a
23 second dielectric layer 21 comprised of a traditional dielectric material such as silicon
24 dioxide. Second dielectric layer 21 together with first dielectric layer 14 isolate low
25 dielectric constant dielectric material 18 from other portions of the integrate circuit. Second
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1 dielectric layer 21 allows further processing, including formation of contact holes for
2 contacting lines of conductive material 16 such as contact hole 46, without exposing
3 dielectric material 18 to processing agents.

4 While the structure shown in Figure 1 results in decreased capacitance between
5 adjacent pairs of metal lines, further decrease is needed to allow increasing miniaturization
6 and high speed operation of ever denser integrated circuits.

SUMMARY OF THE INVENTION

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2 *may* In accordance with the present invention, an interlevel dielectric structure includes
3 first and second dielectric layers between which are located lines of a conductive material
4 with a dielectric material in spaces between the lines of conductive material, with the lower
5 surface of the dielectric material extending lower than the lower surface of lines of
6 conductive material adjacent thereto, and the upper surface of the dielectric material
7 extending higher than the upper surface of lines conductive material adjacent thereto, thus
8 reducing fringe and total capacitance between the lines of conductive material. The dielectric
9 material, which has a dielectric constant of less than about 3.6, does not extend directly
10 above the upper surface of the lines of conductive material, allowing formation of subsequent
11 contacts down to the lines of conductive material without exposing the dielectric material to
12 further processing.

13 A preferred method for forming the interlevel dielectric structure includes providing
14 an additional layer on a conductive layer on a first dielectric layer, then patterning both the
15 additional layer and the conductive layer with an over etch into but not through the first
16 dielectric layer, to form conductive lines with spaces therebetween. A dielectric material is
17 then deposited to fill the spaces and is then etched or chemically mechanically polished back
18 to the additional layer on the conductive layer. The additional layer on the conductive layer
19 is then optionally removed before a second dielectric layer is deposited over all.

20 Another preferred method for forming the interlevel dielectric structure includes
21 providing a conductive layer on a first dielectric layer, then patterning the conductive layer
22 with an over etch into but not through the first dielectric layer to form conductive lines with
23 spaces therebetween. An additional layer is then deposited by a method providing poor step
24 coverage. The additional layer is then optionally etched, and a dielectric material is then
25 deposited in the spaces. The dielectric material is then etched or chemically mechanically
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1 polished back to the additional layer. The additional layer is then optionally removed before
2 a second dielectric layer is deposited over all.

3 Yet another preferred method for forming the interlevel dielectric structure includes
4 providing a metal layer on a first dielectric layer, then patterning the metal layer with an over
5 etch into but not through the first dielectric layer to form metal lines with spaces
6 therebetween. A thin layer of silicon dioxide is then deposited by a method providing
7 preferential deposition on the upper surfaces of the metal lines. The thin layer of silicon
8 dioxide is then optionally etched, and a dielectric material is then deposited to fill the spaces
9 and is then etched or chemically mechanically polished back. A second dielectric layer is
10 then deposited over all.

11 The above briefly described methods allow reliable formation of a desired interlevel
12 dielectric structure, which structure provides reduced total capacitance between adjacent
13 conductive lines needed for further miniaturization of integrated circuits.
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BRIEF DESCRIPTION OF THE DRAWINGS

In order that the manner in which the above-recited and other advantages and objects of the invention are obtained may be more fully explained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments and applications thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments and applications of the invention and are not therefore to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 is a partial cross section of a partially formed integrated circuit device.

Figure 2 is a partial cross section of a partially formed integrated circuit device having a structure formed during the practice of a method of the present invention.

Figure 3 is a partial cross section of a partially formed integrated circuit device for use with a method of the present invention.

Figure 4 is a cross section of the structure shown in Figure 3 after further processing, and having a structure formed by a method of the present invention.

Figure 5 is a partial cross section of a partially formed integrated circuit device showing features formed during the practice of a method of the present invention.

Figure 6 is a partial cross section of a partially formed integrated circuit device depicting facet etching of a bread-loafed dielectric on metallization lines.

Figure 7 is a cross section of the structure shown in Figure 5 after further processing, and having a structure formed by a method of the present invention.

Figure 8 is a partial cross section of a partially formed integrated circuit device showing features formed during the practice of a method of the present invention.

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Figure 9 is a cross section of the structure shown in Figure 8 after further processing, having a structure formed by a method of the present invention.

1 material 16 adjacent thereto, and a lower surface 30 lower than the lower surfaces 24 of lines
2 of conductive material 16 adjacent thereto.

3 The extension of dielectric material 17 below and above lines of conductive material
4 16 significantly reduces capacitance between adjacent pairs of lines of conductive material
5 16.

6 The electric field formed by a potential difference applied across an adjacent pair of
7 lines of conductive material 16 is strongest in a direct line and centrally between the adjacent
8 pair, such as along dashed line N in Figure 2. But the electric field so formed also extends
9 to a fringe area not in a direct line between the adjacent pair, such as along dashed line F in
10 Figure 2. The field in this area, called the fringe, is associated with a portion of the total
11 capacitance, the portion called herein "fringe capacitance," between the adjacent pair.

12 The portion of the total capacitance included in fringe capacitance increases as
13 aspect ratio (height/width) of lines of conductive material 16 decreases, and can be a
14 significant fraction of total capacitance at low aspect ratios. The extension of dielectric
15 material 17 below and above lines of conductive material 16 provides a low dielectric
16 material in the fringe areas of the electric field, thus reducing fringe capacitance and total
17 capacitance accordingly.

18 While dielectric material 17 extends below and above lines of conductive material
19 16, it does not extend directly over surface 26 or under surface 24. This allows formation
20 of contact holes such as contact hole 48 without exposing dielectric material 17 to processing
21 agents that could degrade dielectric material 17 or upper surface 26 at contact hole 48.

22 The above structure and variations thereon may be formed in a variety of ways,
23 presently preferred examples of which will be described below.

24 One preferred method of forming a structure of the present invention includes
25 providing a first dielectric layer 14 over the surface of a substrate of an underling layer 12,
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1 then forming a conductive layer 34 and an additional layer 36 thereover, as shown in
2 Figure 3. Conductive layer 34 and additional layer 36 are then patterned by forming and
3 patterning a mask layer over additional layer 36, and then etching additional layer 36,
4 conductive layer 34, and a portion of first dielectric layer 14 at areas that are left exposed
5 through the mask layer. This results in spaces between adjacent remaining portions of
6 conductive layer 34.

7 Dielectric material 17 is then deposited to fill these spaces, and then removed from
8 the top downward to at least the top of the remaining portions of additional layer 36 by an
9 etch back or by chemical mechanical polishing. A second dielectric layer 21 is then
10 deposited over the substrate, resulting in the structure shown in Figure 4.

11 In Figure 4, lines of conductive material 16 are formed of the remaining portions of
12 conductive layer 34. Dielectric material 17 is deposited between lines of conductive material
13 16. If additional layer 36 is comprised of a suitable dielectric such as silicon dioxide, the
14 remaining portions of additional layer 36 may be incorporated into the inventive structure
15 as shown. Thus the remaining portion of additional layer 36 in Figure 4, together with
16 second dielectric layer 21, correspond to the depiction seen in Figure 2 as second dielectric
17 layer 20.

18 If additional layer 36 is not a dielectric, such as if titanium is used, for example, then
19 the remaining portions of layer 36 shown in Figure 4 are removed by an appropriate process
20 immediately before the deposition of second dielectric layer 20. This alternative additional
21 process step results in a structure like that which is shown in Figure 2.

22 Another preferred method of forming a structure of the present invention includes
23 providing a first dielectric layer over a substrate or an underlying layer, then depositing and
24 patterning a conductive layer over the first dielectric layer. During patterning of the
25 conductive layer, the conductive layer is over etched such that the first dielectric layer is
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1 etched partially with the same pattern. Next, an additional layer is deposited over the
2 patterned metal layer by a deposition method having poor step coverage.

3 The results of the above steps are shown in Figure 5. First dielectric layer 14 has
4 been formed on substrate or underlying layer 12, and a conductive layer has been deposited
5 and patterned, leaving lines of conductive material 16. Additional layer 38 has been
6 deposited by a deposition method having poor step coverage. This results in additional layer
7 38 being formed substantially only on the upper surfaces of lines of conductive material 16
8 as shown.

9 If additional layer 38 is comprised of a suitable dielectric material, the further
10 process steps may proceed as before, with deposition and partial top-down removal of
11 dielectric material 17 and deposition of second dielectric layer 21, resulting in the structure
12 shown in Figure 7. The remaining portions of additional layer 38 are incorporated into the
13 inventive structure as shown, so that the remaining portion of additional layer 38 in Figure
14 5 together with second dielectric layer 21 in Figure 7, correspond to the depiction seen in
15 Figure 2 as second dielectric layer 20.

16 Silicon dioxide is the currently preferred material for additional layer 38, with
17 deposition by a silane and oxygen plasma enhanced chemical vapor deposition (PECVD)
18 being the preferred poor step coverage deposition method.

19 Figure 6 illustrates an optional etch step that may be included immediately after
20 deposition of additional layer 38 to remove lateral buildup of additional layer 38. The
21 preferred etch is a facet etch, and is preferably performed in an argon or an argon-plus-
22 fluorine based plasma. In a facet etch, additional layer 38 is etched slower at a top surface
23 thereof than it is etched at a corner thereof which connects the top surface to a lateral surface
24 thereof. The facet etch has the effect of removing substantially all of the lateral buildup
25 portions of additional layer 38 and the removed portions redeposit in semi-triangular form
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1 at the base of the lines of conductive material 16 and first dielectric layer 14 interface. A
2 continuous but thin lateral layer of additional layer 38 also deposits down the sides of lines
3 of conductive material 16. Further processing as above then results in a structure like that
4 which is shown in Figure 4, with the remaining portions of layer of additional material 36
5 corresponding to the remaining portions of additional layer 38. The redeposited fraction of
6 additional material 38, however, remains thinly on the sides of lines of conductive material
7 16 and first dielectric layer 14.

8 If additional layer 38 is not a dielectric, or is otherwise not suitable to remain in
9 place in the inventive structure, then additional layer 38 is removed by an appropriate process
10 immediately before the deposition of second dielectric layer 21. This alternative additional
11 process step results in a structure that is like that shown in Figure 2.

12 In yet another presently preferred method for forming a structure of the present
13 invention, a first dielectric layer is provided over a substrate or an underlying layer, then a
14 metal layer is deposited and patterned to form metal lines over the first dielectric layer.
15 During patterning of the metal layer, the metal layer is over etched such that the first
16 dielectric layer is etched partially with the same pattern. A thin silicon dioxide layer is then
17 deposited conformably over the metal lines by a deposition process that deposits
18 preferentially on the upper surface of the metal lines.

19 The above process results generally in the structure shown in Figure 8. First
20 dielectric layer 14 is formed on substrate 12. Metal lines in the preferred form of aluminum
21 lines 40 have been formed on first dielectric layer 14, and first dielectric layer 14 has been
22 over etched in the same pattern as aluminum lines 40. A titanium nitride film 42 from a
23 photolithography process used to pattern aluminum lines 40 remains on the upper surface of
24 aluminum lines 40. While not required, inclusion of titanium nitride film 42 is presently
25 preferred.
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1 The preferred deposition process for selectively depositing a thin silicon dioxide
2 layer 44 is an ozone based TEOS process, which preferentially deposits on TiN over silicon
3 dioxide. Preferably, silicon dioxide layer 44 will be deposited only on titanium nitride
4 film 42 and not on the sidewall of aluminum lines 40 as shown in Figure 8.

5 After deposition of silicon dioxide layer 44, the process may continue as with the
6 other above processes by deposition and partial removal of a dielectric material 17, followed
7 by deposition of second dielectric layer 21, resulting in the structure shown in Figure 9.
8 Silicon dioxide layer 44 is incorporated into the inventive structure as shown, so that silicon
9 dioxide layer 44 together with second dielectric layer 21 correspond to the depiction seen in
10 Figure 2 as second dielectric layer 20.

11 As an alternative process step, an etch such as a facet etch in an argon or an argon-
12 plus-fluorine based plasma may be performed on silicon dioxide layer 44 after the deposition
13 thereof.

14 The present invention may be embodied in other specific forms without departing
15 from its spirit or essential characteristics. The described embodiments are to be considered
16 in all respects only as illustrated and not restrictive. The scope of the invention is, therefore,
17 indicated by the appended claims and their combination in whole or in part rather than by the
18 foregoing description. All changes which come within the meaning and range of equivalency
19 of the claims are to be embraced within their scope.

20 What is claimed and desired to be secured by United States Letters Patent is:
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Abstract

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1. A method of forming an interlevel dielectric comprising the steps of:

- providing a first dielectric layer over a surface of a substrate situated on a semiconductor wafer;
- depositing a conductive layer on said first dielectric layer;
- depositing an additional layer on said conductive layer;
- patterning said conductive layer and said additional layer by
 - forming a patterned mask layer on said additional layer, and
 - etching through said additional layer and said conductive layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material;
- depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space;
- removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and
- depositing a second dielectric layer over all layers on said surface of said substrate.

2. The method as defined in Claim 1, further comprising the step, to be performed after said step of removing said layer of dielectric material and before said step of depositing a second dielectric layer, of removing said additional layer on said lines of conductive material.

3. The method as defined in Claim 2, wherein said additional layer comprises titanium.

Run	Time	Temp	Pressure	Flow	Conc	Yield	Quality
1	10:00	25.0	1.0	1.0	1.0	1.0	1.0
2	10:15	25.0	1.0	1.0	1.0	1.0	1.0
3	10:30	25.0	1.0	1.0	1.0	1.0	1.0
4	10:45	25.0	1.0	1.0	1.0	1.0	1.0
5	11:00	25.0	1.0	1.0	1.0	1.0	1.0
6	11:15	25.0	1.0	1.0	1.0	1.0	1.0
7	11:30	25.0	1.0	1.0	1.0	1.0	1.0
8	11:45	25.0	1.0	1.0	1.0	1.0	1.0
9	12:00	25.0	1.0	1.0	1.0	1.0	1.0
10	12:15	25.0	1.0	1.0	1.0	1.0	1.0
11	12:30	25.0	1.0	1.0	1.0	1.0	1.0
12	12:45	25.0	1.0	1.0	1.0	1.0	1.0
13	13:00	25.0	1.0	1.0	1.0	1.0	1.0
14	13:15	25.0	1.0	1.0	1.0	1.0	1.0
15	13:30	25.0	1.0	1.0	1.0	1.0	1.0
16	13:45	25.0	1.0	1.0	1.0	1.0	1.0
17	14:00	25.0	1.0	1.0	1.0	1.0	1.0
18	14:15	25.0	1.0	1.0	1.0	1.0	1.0
19	14:30	25.0	1.0	1.0	1.0	1.0	1.0
20	14:45	25.0	1.0	1.0	1.0	1.0	1.0
21	15:00	25.0	1.0	1.0	1.0	1.0	1.0
22	15:15	25.0	1.0	1.0	1.0	1.0	1.0
23	15:30	25.0	1.0	1.0	1.0	1.0	1.0
24	15:45	25.0	1.0	1.0	1.0	1.0	1.0
25	16:00	25.0	1.0	1.0	1.0	1.0	1.0
26	16:15	25.0	1.0	1.0	1.0	1.0	1.0
27	16:30	25.0	1.0	1.0	1.0	1.0	1.0
28	16:45	25.0	1.0	1.0	1.0	1.0	1.0
29	17:00	25.0	1.0	1.0	1.0	1.0	1.0
30	17:15	25.0	1.0	1.0	1.0	1.0	1.0
31	17:30	25.0	1.0	1.0	1.0	1.0	1.0
32	17:45	25.0	1.0	1.0	1.0	1.0	1.0
33	18:00	25.0	1.0	1.0	1.0	1.0	1.0
34	18:15	25.0	1.0	1.0	1.0	1.0	1.0
35	18:30	25.0	1.0	1.0	1.0	1.0	1.0
36	18:45	25.0	1.0	1.0	1.0	1.0	1.0
37	19:00	25.0	1.0	1.0	1.0	1.0	1.0
38	19:15	25.0	1.0	1.0	1.0	1.0	1.0
39	19:30	25.0	1.0	1.0	1.0	1.0	1.0
40	19:45	25.0	1.0	1.0	1.0	1.0	1.0
41	20:00	25.0	1.0	1.0	1.0	1.0	1.0
42	20:15	25.0	1.0	1.0	1.0	1.0	1.0
43	20:30	25.0	1.0	1.0	1.0	1.0	1.0
44	20:45	25.0	1.0	1.0	1.0	1.0	1.0
45	21:00	25.0	1.0	1.0	1.0	1.0	1.0
46	21:15	25.0	1.0	1.0	1.0	1.0	1.0
47	21:30	25.0	1.0	1.0	1.0	1.0	1.0
48	21:45	25.0	1.0	1.0	1.0	1.0	1.0
49	22:00	25.0	1.0	1.0	1.0	1.0	1.0
50	22:15	25.0	1.0	1.0	1.0		

The method as defined in Claim 1, wherein said conductive material is selected from the group consisting of polysilicon, aluminum, copper, tungsten, and multiple layers of TiN/Al/TiN, TiN/Al/Ti, W/TiN/Ti, or any combinations thereof.

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1 11. A method of forming an interlevel dielectric comprising the steps of:
2 providing a first dielectric layer over a surface of a substrate situated on a
3 semiconductor wafer;
4 depositing a conductive layer on said first dielectric layer;
5 patterning said conductive layer by
6 forming a mask layer on said conductive layer, and
7 etching through said conductive layer and into said first dielectric
8 layer, leaving a space between adjacent remaining portions of said conductive
9 layer, said adjacent remaining portions of said conductive layer forming lines
10 of conductive material each having an upper surface;
11 depositing an additional layer on the upper surfaces of lines of conductive
12 material and on said first dielectric layer;
13 depositing a layer of dielectric material having a dielectric constant of less
14 than about 3.6 to fill said space;
15 removing said layer of dielectric material from the top thereof downward to
16 at least to the level of the top of said additional layer; and
17 depositing a second dielectric layer over all layers on said surface of said
18 substrate.

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20 12. The method as defined in Claim 11, wherein depositing an additional layer
21 comprises depositing a layer of silicon dioxide by silane and oxygen based plasma
22 enhanced chemical vapor deposition.
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- 1 13. The method as defined in Claim 11, further comprising, after depositing an
2 additional layer and before depositing a layer of dielectric material, of etching said
3 additional layer.
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- 5 14. The method as defined in Claim 13, wherein said additional layer has a top surface
6 extending to a lateral surface at a corner, and wherein said step of performing an
7 etch on said additional layer etches the corner of the additional layer faster than the
8 top surface of the additional layer.
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- 10 15. The method as defined in Claim 13, wherein said additional layer comprises silicon
11 dioxide and wherein said step of performing an etch on said additional layer etches
12 in an argon or an argon-plus-fluorine based plasma.
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- 14 16. The method as defined in Claim 11, wherein at least one of said first and second
15 dielectric layers comprises silicon dioxide.
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- 17 17. The method as defined in Claim 11, wherein said dielectric material comprises
18 PTFE.
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- 20 18. The method as defined in Claim 11, wherein said additional layer comprises silicon
21 dioxide.
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- 23 19. The method as defined in Claim 11, wherein said step of removing said layer of
24 dielectric material comprises an etch back step.
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20. The method as defined in Claim 11, wherein said step of removing said layer of dielectric material comprises a chemical mechanical polishing step.
21. The method as defined in Claim 11, wherein said conductive material is selected from the group consisting of polysilicon, aluminum, and copper.
22. A method of forming an interlevel dielectric comprising the steps of:
- providing a first dielectric layer over a surface of a substrate situated on a semiconductor wafer;
 - depositing a metal layer on said first dielectric layer;
 - patterning said metal layer by
 - forming a mask layer on said metal layer, and
 - etching through said metal layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said metal layer, said adjacent remaining portions of said metal layer forming metal lines each having an upper surface;
 - depositing a thin layer of silicon dioxide conformably over said metal lines and selectively on said upper surfaces of said metal lines;
 - depositing a layer of dielectric material having a dielectric constant of less than about 3.6 to fill said space;
 - removing said layer of dielectric material from the top thereof downward to at least to the level of the top of said additional layer; and
 - depositing a second dielectric layer over all layers on said surface of said substrate.

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- Docket No. 11675.76.1.1

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35. A method of forming an interlevel dielectric comprising:

- providing a first dielectric layer over a surface of a substrate;
- forming a conductive layer on said first dielectric layer;
- forming an additional layer on said conductive layer;
- etching through said additional layer and said conductive layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material;
- filling the spaces between adjacent remaining portions of said conductive layer with dielectric material having a dielectric constant of less than about 3.6;
- forming a second dielectric layer on the additional layer.

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